AMENDMENT TO THE CLAIMS

1. (Currently amended) An error portion detecting method for a semiconductor integrated circuit, comprising:

a transition timing detecting step of detecting a transition timing of an input signal input to, or a transition timing of an output signal output from, each of circuit elements which are supplied with a supply voltage through a common power supply line;

a simultaneous-operation circuit element number detecting step of detecting a number of circuit elements in which the transition timing of the input signal or output signal occurs within a predetermined time interval;

a supply voltage variation level estimating step of estimating a supply voltage variation level based on the number of circuit elements which is detected at the simultaneous-operation circuit element number detecting step; and

an outputting step of outputting the estimated supply voltage variation level.

2. (Previously presented) The error portion detecting method of claim 1, wherein the supply voltage variation level estimating step includes a step of estimating the supply voltage variation level based on a variation of the transition timings detected at the transition timing detecting step.

3. (Original) The error portion detecting method of claim 1, wherein the circuit elements are transistors.

4. (Original) The error portion detecting method of claim 1, wherein the circuit elements are buffer circuits.

5. (Previously presented) The error portion detecting method of claim 1, wherein:

the circuit elements are scan flip-flops for testing an operation of the semiconductor integrated circuit; and

the input signal is a clock signal which is input to the scan flip-flops.

6. (Previously presented) The error portion detecting method of claim 1, wherein the transition timing detecting step includes a step of detecting the transition timing of the input signal or output signal by simulating an operation of the semiconductor integrated circuit.

7. (Previously presented) The error portion detecting method of claim 1, wherein the transition timing detecting step includes a step of detecting the transition timing of the input signal or output signal based on a delay time caused by a circuit element and signal line for transmitting the input signal to each of the circuit elements.

8. (Currently amended) An error portion detecting method for a semiconductor integrated circuit, comprising:

a circuit element number detecting step of detecting a number of circuit elements which are supplied with a supply voltage through a common power supply line and in

which input signals are supposed to simultaneously transition when a delay caused by a signal line is neglected;

a supply voltage variation level estimating step of estimating a supply voltage variation level based on the number detected at the circuit element number detecting step; and

an outputting step of outputting the estimated supply voltage variation level..

9. (Previously presented) A layout method for a semiconductor integrated circuit, comprising:

a transition timing detecting step of detecting a transition timing of an input signal input to, or a transition timing of an output signal output from, each of circuit elements which are supplied with a supply voltage through a common power supply line;

a simultaneous-operation circuit element number detecting step of detecting a number of circuit elements in which the transition timing of the input signal or output signal occurs within a predetermined time interval; and

a configuration determining step of determining a configuration of the circuit elements or a configuration of power supply lines based on the number of circuit elements which is detected at the simultaneous-operation circuit element number detecting step, such that any of the circuit elements is supplied with the supply voltage through a power supply line different from the common power supply line.

10. (Currently amended) A computer-readable medium storing an error portion detecting program for a semiconductor integrated circuit which instructs a

computer to execute the following steps:

a transition timing detecting step of detecting a transition timing of an input signal input to, or a transition timing of an output signal output from, each of circuit elements which are supplied with a supply voltage through a common power supply line;

a simultaneous-operation circuit element number detecting step of detecting a number of circuit elements in which the transition timing of the input signal or output signal occurs within a predetermined time interval;

a supply voltage variation level estimating step of estimating a supply voltage variation level based on the number of circuit elements which is detected at the simultaneous-operation circuit element number detecting step; and

an outputting step of outputting the estimated supply voltage variation level.

11. (Previously presented) A computer-readable medium storing a layout program for a semiconductor integrated circuit which instructs a computer to execute the following steps:

a transition timing detecting step of detecting a transition timing of an input signal input to, or a transition timing of an output signal output from, each of circuit elements which are supplied with a supply voltage through a common power supply line;

a simultaneous-operation circuit element number detecting step of detecting a number of circuit elements in which the transition timing of the input signal or output signal occurs within a predetermined time interval; and

a configuration determining step of determining a configuration of the circuit elements or a configuration of power supply lines based on the number of circuit

elements which is detected at the simultaneous-operation circuit element number detecting step, such that any of the circuit elements is supplied with the supply voltage through a power supply line different from the common power supply line.